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54 Frequency difference detector (FDD) having automatic gain control and a carrier modulated receiver including the FDD.

57 A frequency difference detector (FDD) implemented as a balanced quadricorrelator has an automatic gain control system (68) having inputs capacitively coupled to the quadrature related, baseband frequency paths from the front end mixers (12,14). The a.g.c. system (68) has quadrature related mixers (78,80) coupled to said inputs for frequency up-converting the baseband signals to an intermediate frequency. The IF signals from the mixers are summed in a summing circuit (82) and subsequently squared in a squaring circuit (86). Any ripple in the output of the squaring circuit is removed by low pass filtering to produce a d.c. control signal which is applied to gain controlled amplifiers (22,24) present in said baseband frequency paths in order to render the output (V_o) of the FDD less sensitive to variations in the input signal (V_i).

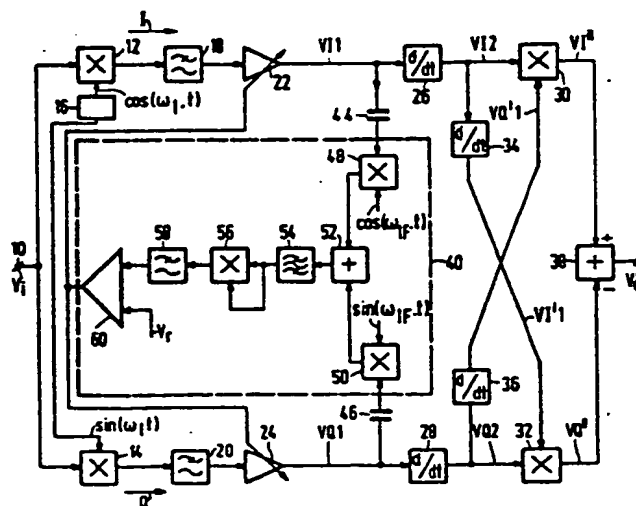


FIG.1

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Frequency Difference Detector (FDD) having automatic gain control and a carrier modulated receiver including the FDD

The present invention relates to a frequency difference detector (FDD) having automatic gain control and to a carrier modulated receiver including the FDD.

In carrier modulated receivers it is essential for the local oscillator frequency to track the transmitted carrier frequency so that the difference between the two frequencies is set to within a tolerable accuracy. Automatic frequency control (AFC) circuits are normally used for deriving a measure of this difference in frequency and for automatically adjusting the local oscillator. Consequently a frequency difference detector forms the heart of all AFC loops and can be realised in various forms. The particular FDD of interest in the present application is termed a balanced quadricorrelator. A known type of balanced quadricorrelator is shown in Figure 3 of an article "Properties of Frequency Difference Detectors" by Floyd M Gardner, IEEE Transactions on Communications, Vol COM 33 No 2, February 1985, Pages 131 to 138. The known circuit comprises quadrature related, first and second mixers in which an input signal is mixed down to I and Q baseband signals. Low pass filters are provided in the output circuits of the first and second mixers in order to select the in-band signal components. The output of one of the low pass filters is (1) applied to an input of a third mixer and (2) differentiated and applied to an input of a fourth mixer. The output of the other of low pass filters is (1) applied to another input of the third mixer and (2) differentiated and applied to another input of the fourth mixer. The outputs of the third and fourth mixers are subtracted from each other to provide a frequency difference signal. It can be shown that the output voltage V_d of such a balanced quadricorrelator is proportional to the frequency difference $\Delta\omega$ between the transmitted carrier and the local oscillator and is given by

$$V_d \propto E \cdot \Delta\omega$$

where E is the amplitude of the input signal. It is evident from this equation that the detected output voltage is highly sensitive to the amplitude E of the input signal which is a shortcoming of this type of circuit.

A.g.c. systems for balanced quadricorrelator circuits are known, for example from Japanese Kokai 58-137309. In the known a.g.c. system the signals from the low pass filters in the two signals paths are applied to gain controlled amplifiers and the outputs therefrom are squared and summed to produce a signal freed of modulation. This signal is applied as a control signal to the gain controlled amplifiers. Such an arrangement is not optimum because the multipliers used in squaring the signals from the gain controlled amplifiers suffer from a dynamic range problem due to accumulated d.c. offsets in the mixers and gain controlled amplifiers.

It is an object of the present invention to provide an improved automatic gain control system for FDD's.

According to the present invention there is provided a frequency difference detector comprising means for producing quadrature related first and second baseband signals, means for selecting in-band signal components in said first and second baseband signals, variable gain amplifying means responsive to an a.g.c. signal for adjusting the amplitude of the in-band signal components, and an a.g.c. system for providing said a.g.c. signal, said a.g.c. system comprising first and second inputs capacitively coupled to signal paths carrying the in-band signal components of the quadrature related first and second signals, first and second quadrature related mixers for frequency up-converting the signals on the first and second inputs, respectively, means for summing said frequency up-converted signals, means for squaring the summed signal and means for deriving an a.g.c. signal from the squared signal and for applying the a.g.c. signal to the variable gain amplifying means.

The present invention also provides a frequency difference detector comprising a signal input terminal, a local oscillator, first and second mixers, means coupling the signal input terminal to first inputs of the first and second mixers and the local oscillator to second inputs of the first and second mixers, a 90° phase shifter provided in the signal/local oscillator path to one of the inputs of the first and second mixers whereby the first and second mixers produce first and second orthogonally related outputs, respectively, first and second frequency selecting means provided in the output circuits of the first and second mixers, respectively, a first electrical path connecting the first frequency selecting means to a first input of a third mixer, a second electrical path connecting the first frequency selecting means to a second input of a fourth mixer, a third electrical path connecting the second frequency selecting means to a first input of a fourth mixer, a fourth electrical path connecting the second frequency selecting means to a second input of the third mixer, differential means provided in the second and fourth electrical paths, signal subtracting means

connected to outputs of the third and fourth mixers, first and second adjustable gain amplifiers connected respectively in first and second signal branches between the input terminal and the third and fourth mixers and an automatic gain control circuit comprising fifth and sixth mixers having first inputs capacitively connected to the first and second branches, respectively, second inputs of the fifth and sixth mixers being
 5 connected to quadrature related outputs of an intermediate frequency local oscillator, summing means for summing the outputs of the fifth and sixth mixers, a signal squaring means coupled to the output of the summing means and a low pass filtering means for passing at least the d.c. component of the output signal from the squaring means, which d.c. component comprises a gain control signal for the first and second adjustable gain amplifiers.

10 In the FDD made in accordance with the present invention the problem of d.c. offsets in the signals applied to the a.g.c. system is mitigated by using capacitors. Additionally unlike the known a.g.c. system in which the baseband signals are square, the a.g.c. signal is derived from a remodulated signal at an intermediate frequency. The specification of the fifth and sixth mixers used for the quadrature remodulation of the baseband signals is not critical because the summed output from these mixers is used only for
 15 deriving a measure of the input signal strength and not for demodulation.

If desired a bandpass filter may be connected between the summing means for summing the outputs of the fifth and sixth mixers and the signal squaring means. The envelope of the signal at the output of the bandpass filter is representative of the input signal amplitude E.

The present invention will now be described, by way of example, with reference to the accompanying
 20 drawings, wherein:

Figure 1 is a block schematic circuit of a first embodiment of a FDD made in accordance with the present invention,

Figure 2 illustrates a digital demodulator, and

Figure 3 is a block schematic circuit of a second embodiment of a FDD made in accordance with the
 25 present invention.

In the drawings the same reference numerals have been used to indicate the corresponding features.

The FDD shown in Figure 1 comprises a quadrature front end comprising first and second mixers 12, 14 having inputs connected to an input terminal 10 and to a local oscillator. Outputs from the mixers 12, 14
 30 are quadrature related and in the illustrated embodiment this is carried out by phase shifting the local oscillator signal applied to the second mixer 14. Alternatively a 90° phase shifter could be connected between the input terminal 10 and signal input to the first or second mixer. The local oscillator frequency may be the same as or slightly different from the carrier frequency of an input signal V_i . Low pass filters 18, 20 select the difference components in the outputs of the first and second mixers 12, 14. The filtered
 35 signals have their amplitudes adjusted by adjustable gain amplifiers 22, 24 and produce signals V_{I1} and V_{Q1} , where I means in-phase and Q means quadrature phase. The signals V_{I1} and V_{Q1} are differentiated once in differential circuits 26, 28, respectively, and applied to first inputs of third and fourth mixers 30, 32 as signals V_{I2} and V_{Q2} , respectively. These signals V_{I2} and V_{Q2} are differentiated in differential circuits 34, 36 and applied as signals $V_{I'1}$ and $V_{Q'1}$ to second inputs of the fourth and third mixers 32, 30, respectively. The outputs $V_{I''}$ and $V_{Q''}$ are applied to a subtracting circuit 38 which produces an output
 40 signal V_o .

By differentiating the signals applied to both inputs of the third and fourth mixers any d.c. offset voltages are blocked because "differentiation" is a high pass junction. Thus the dynamic range of these mixers 30, 32 will not be affected by the accumulated offsets in the preceding circuit stages. The only d.c.
 45 offset voltages which could appear in the output signal V_o are those due to the mixers 30, 32 and the subtracting circuit 38. It is necessary to ensure that there is one order difference between the differentiated signals applied to the first inputs of the mixers 30, 32 and those applied to the second inputs of the same mixers.

The signals at the various points of Figure 1 are given as follows:

$$\begin{aligned}
 50 \quad V_i &= E \cdot \cos(\omega_i t) \\
 V_{I1} &= \frac{E}{2} \cdot \cos(\Delta\omega t) \\
 V_{I2} &= \frac{E}{2} \cdot \Delta\omega \cdot \sin(\Delta\omega t) \\
 V_{I'1} &= -\frac{E}{2} [\sin(\Delta\omega t) \cdot \frac{d(\Delta\omega)}{dt} + \Delta\omega^2 \cdot \sin(\Delta\omega t)] \\
 V_{Q1} &= \frac{E}{2} \cdot \sin(\Delta\omega t) \\
 55 \quad V_{Q2} &= \frac{E}{2} \cdot \Delta\omega \cdot \cos(\Delta\omega t) \\
 V_{Q'1} &= \frac{E}{2} [\cos(\Delta\omega t) \cdot \frac{d(\Delta\omega)}{dt} - \Delta\omega^2 \cdot \sin(\Delta\omega t)]
 \end{aligned}$$

$$VI'' = -\frac{E^2}{4} [\Delta\omega \sin(\Delta\omega t) \cos(\Delta\omega t) \cdot \frac{d(\Delta\omega)}{dt} - (\Delta\omega)^3 \sin^2(\Delta\omega t)]$$

$$VQ'' = -\frac{E^2}{4} [\Delta\omega \sin(\Delta\omega t) \cos(\Delta\omega t) \cdot \frac{d(\Delta\omega)}{dt} + (\Delta\omega)^3 \cos^2(\Delta\omega t)]$$

$$V_0 = VI'' - VQ'' = \frac{E^2}{4} \cdot (\Delta\omega)^3 \propto E^2 (\Delta\omega)^3$$

Where E is amplitude and $\Delta\omega$ is the frequency difference between the transmitted carrier ω_1 and the local oscillator ω_2 , such that $\Delta\omega = (\omega_1 - \omega_2)$. The final equation for V_0 shows that the output of the FDD is now proportional to $(\Delta\omega)^3$, instead of $(\Delta\omega)$ as with an conventional balanced quadricorrelator. This change in output for a given change in frequency difference ($\Delta\omega$) associated with the embodiment of Figure 1 is much greater and is a desirable characteristic. Such a characteristic reduces the remaining problems of d.c. offsets due to the third and fourth mixers 30, 32 and the subtracting circuits 38.

Provided that there is a difference of one differential order between the inputs to each of the third and fourth mixers 30, 32 then various arrangements of differential circuits are possible in order to ensure that the inputs to the third and fourth mixers 30, 32 are free of d.c. offsets. A limiting factor in selecting an arrangement is that differentiation is a noise enhancement process and in practice a compromise has to be made having regard to circuit complexity and noise consideration.

It will be recalled that the output signal V_0 from the subtracting circuit 38 (Figure 1) contains a term in E^2 where E is the input voltage to the FDD. In order to make V_0 less sensitive to variations in the input signal V_i an automatic gain control (a.g.c.) system 40 is provided in the FDD shown in Figure 1. The adjustable gain amplifiers 22, 24 are provided in the I and Q signal paths at appropriate signal points. The positions shown at the outputs of the low pass filters 18, 20 are only exemplary in order to illustrate the operating principle.

The inputs to the a.g.c. circuit 40 comprise the signals VI_1 and VQ_1 which are coupled via capacitors 44, 46 to mixers 48, 50 in which they are frequency up-converted to an intermediate frequency (IF) of say 100 KHz which is applied in quadrature to these mixers 48, 50. The outputs of the mixers 48, 50 are combined in a summing circuit 52. The combined signal is band pass filtered in a filter 54 and the output signal therefrom is squared, that is multiplied by itself, in a multiplier 56. A low pass filter 58 is connected to the multiplier 56 to remove ripple due to modulation and provide a d.c. signal. The output from the low pass filter 58 is applied to an op-amp 60 to which a reference voltage V_r is applied. The output voltage from the op-amp 60 comprises the d.c. gain control signal for the amplifiers 22, 24.

The squaring of the signal from the band pass filter 54 may alternatively have been carried out using a rectifier or a logarithmic amplifier.

The FDD can be used as a demodulator for a FM signal. However since the output signal V_0 of the FDD is not linearly related to the frequency difference of the input signal V_i , V_0 being proportional to $(\Delta\omega)^3$, an extra signal processing step is needed to recover the original modulation.

The equation for the output V_0 of the FDD can be rewritten as follows:

$$V_0 = K(\Delta\omega)^3 = K(\omega_c + \omega_m)$$

where ω_c is a constant frequency difference, and ω_m is the instantaneous frequency produced by the modulating signal, and

K is a gain constant.

The desired modulation can now be recovered by processing V_0 of the preceding equation with a cube root function. This can be done digitally or by analogue signal processing. However a cube root function is not an easy function to realise and a digital embodiment will be described with reference to Figure 2.

The FDD output signal V_0 is low pass filtered in a filter 62 and applied to an analogue-to-digital converter 64 which is clocked by clock signals on a line 65. The digitised output is applied to a read only memory (ROM) 66 which serves as a look-up table for the required cube root function, namely

$$[V_0]^{1/3} = \text{Exp}\left[\frac{\text{sign}(V_0)}{3} \cdot \ln(|V_0|)\right]$$

The output of the ROM 66 is applied to a digital-to-analogue converter 68 which provides an analogue cube

root signal which is low pass filtered in a filter 70 to provide an output formed by the modulating signal.

The use of the described FDD as an FM demodulator provides two advantages over conventional dual branch architecture thereby reducing the output distortion. These two advantages are:

- (1) The problem of "hole-in-spectrum" caused by a.c. coupling is avoided.
- (2) The cross-coupling of the two branches suggests that deviations in gain and phase of the two branches could be balanced-out thus reducing distortion and interference in the audio output caused by these imperfections.

Referring to Figure 3 which illustrates another embodiment of an FDD having automatic gain control. The basic FDD circuit without the a.g.c. system 40 is known per se and is disclosed for example in Figure 3 of an article "Properties of Frequency Difference Detectors" by Floyd M. Gardner, IEEE Transactions on Communications, Vol. COM 33, No. 2, February 1985, pages 131 to 138. The difference between the embodiment shown in Figure 1 and that shown in Figure 3 is that the signal inputs to the first inputs of the third and fourth mixers 30,32 have not been differentiated or high pass filtered so that these signals contain d.c. offsets which have been accumulated in the preceding processing steps in the FDD.

Nevertheless the output signal V_o does contain a term in E^2 and in consequence the output signal is sensitive to amplitude changes in the input signal. Providing the a.g.c. system 40 reduces this sensitivity of the output signal to changes in the input signal V_i . As the a.g.c. system has been described in full with reference to Figure 1, it will not be repeated.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of FDDs and carrier modulated receivers and component parts thereof and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or any further application derived therefrom.

Claims

1. A frequency difference detector comprising means for producing quadrature related first and second baseband signals, means for selecting in-band signal components in said first and second baseband signals, variable gain amplifying means responsive to an a.g.c. signal for adjusting the amplitude of the in-band signal components, and an a.g.c. system for providing said a.g.c. signal, said a.g.c. system comprising first and second inputs capacitively coupled to signal paths carrying the in-band signal components of the quadrature related first and second signals, first and second quadrature related mixers for frequency up-converting the signals on the first and second inputs, respectively, means for summing said frequency up-converted signals, means for squaring the summed signal and means for deriving an a.g.c. signal from the squared signal and for applying the a.g.c. signal to the variable gain amplifying means.

2. A frequency difference detector comprising a signal input terminal, a local oscillator, first and second mixers, means coupling the signal input terminal to first inputs of the first and second mixers and the local oscillator to second inputs of the first and second mixers, a 90° phase shifter provided in the signal/local oscillator path to one of the inputs of the first and second mixers whereby the first and second mixers produce first and second orthogonally related outputs, respectively, first and second frequency selecting means provided in the output circuits of the first and second mixers, respectively, a first electrical path connecting the first frequency selecting means to a first input of a third mixer, a second electrical path connecting the first frequency selecting means to a second input of a fourth mixer, a third electrical path connecting the second frequency selecting means to a first input of a fourth mixer, a fourth electrical path connecting the second frequency selecting means to a second input of the third mixer, differential means provided in the second and fourth electrical paths, signal subtracting means connected to outputs of the third and fourth mixers, first and second adjustable gain amplifiers connected respectively in first and second signal branches between the input terminal and the third and fourth mixers and an automatic gain control circuit comprising fifth and sixth mixers having first inputs capacitively connected to the first and

second branches, respectively, second inputs of the fifth and sixth mixers being connected to quadrature related outputs of an intermediate frequency local oscillator, summing means for summing the outputs of the fifth and sixth mixers, a signal squaring means coupled to the output of the summing means and a low pass filtering means for passing at least the d.c. component of the output signal from the squaring means.

5 which d.c. component comprises a gain control signal for the first and second adjustable gain amplifiers.
3. A detector as claimed in claim 2, wherein a bandpass filter is connected between the summing means and the signal squaring means.

4. A detector as claimed in claim 2 or 3, wherein differential means are provided in the first and third electrical paths and wherein the differential means in the first and third electrical paths are one order
10 different compared to the differential means in the second and fourth electrical paths.

5. A detector as claimed in claim 4, wherein at least one differential means in the first and second electrical paths is common to both said paths and at least one differential means in the third and fourth electrical paths is common to both said paths.

6. A frequency difference detector as claimed in claim 1 or 2, constructed and arranged to operate with
15 reference to and as shown in the accompanying drawings.

7. A carrier modulated receiver having an FM demodulator including the frequency difference detector (FDD) as claimed in any one of claims 1 to 6.

8. A receiver as claimed in claim 7, wherein the output signal of the FDD comprises a cubic function and wherein the modulating signal is recovered by obtaining the cube root of the said function.

20 9. A receiver as claimed in claim 8, wherein the output of the FDD is applied to a digital cube root circuit comprising an analogue to digital converter having outputs connected to a look-up table containing cube roots of the said function, and a digital to analogue converter coupled to the look-up table and having an output for the modulating signal.

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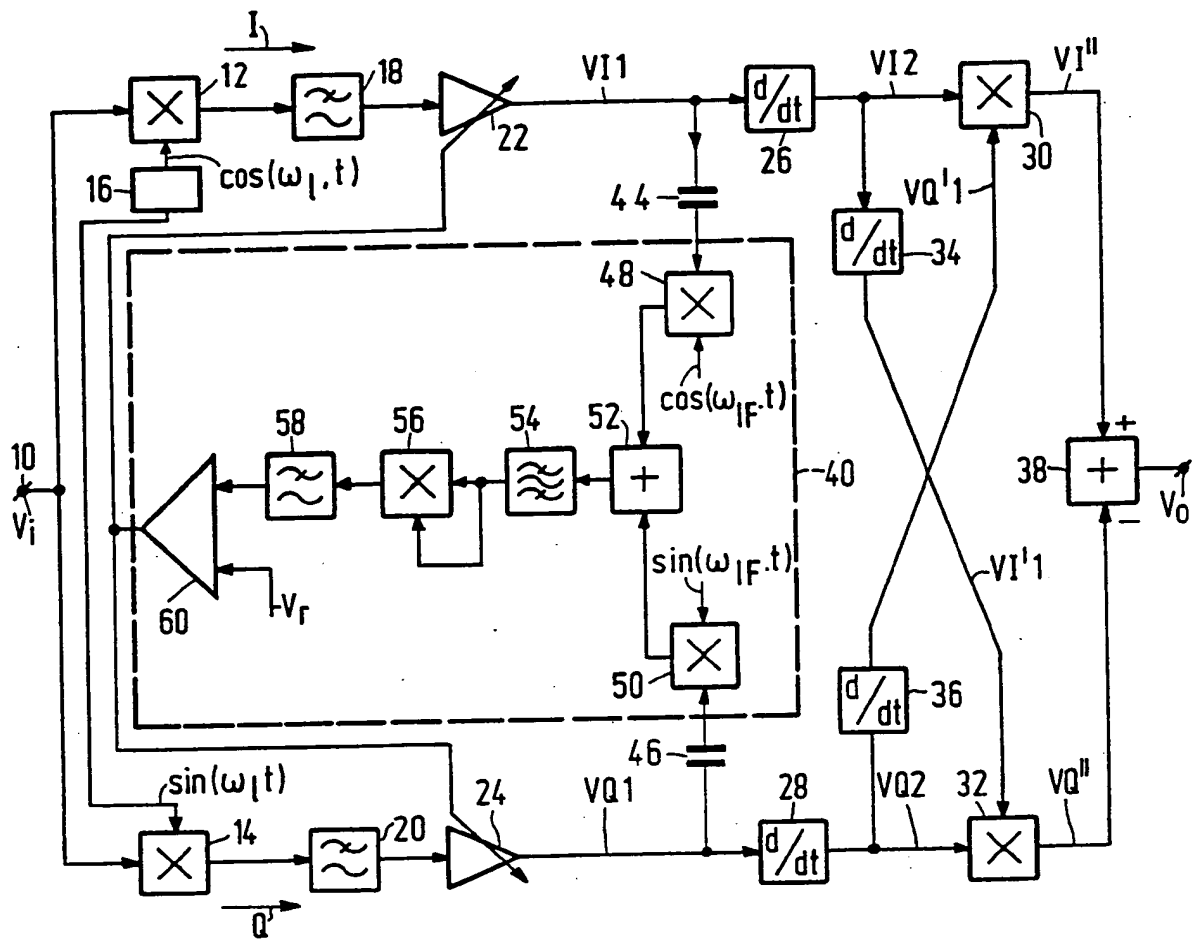


FIG.1

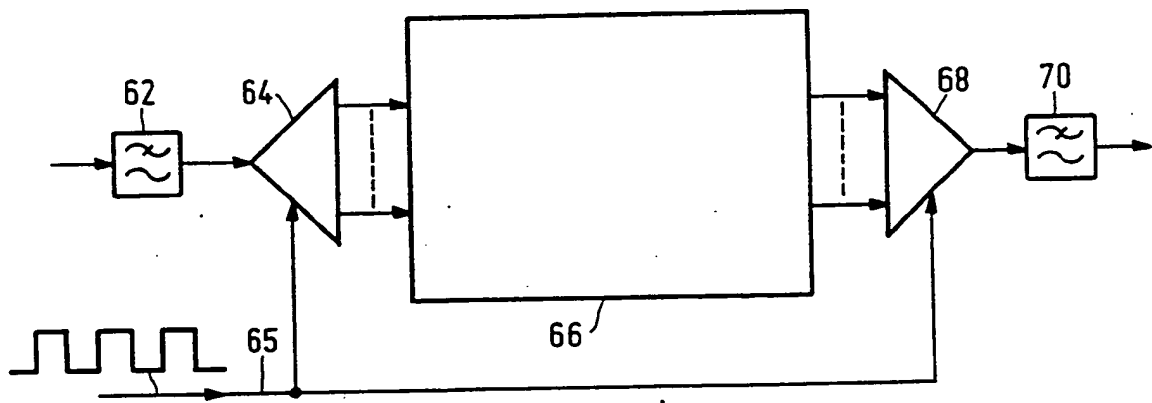


FIG.2

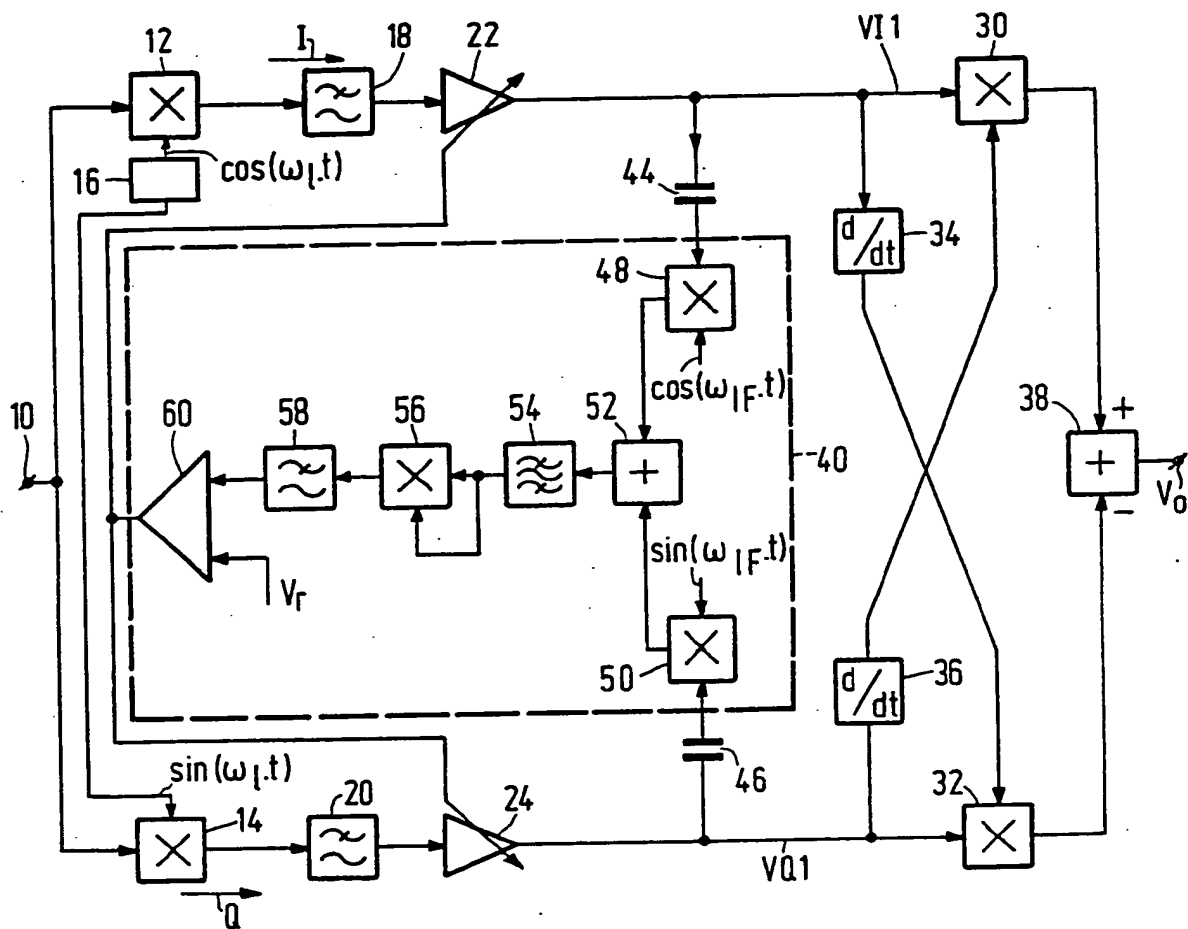


FIG.3



European Patent
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EUROPEAN SEARCH REPORT

Application Number

EP - 88 20 2103

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | |
|---|---|--|---|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. CL 4) |
| A | DE-A-2 800 242 (HIRADASTECHNIKAI IPARI KUTATO INTEZET) * Page 14, lines 3-22; page 18, line 12 - page 21, line 10; figure 4 * | 1,2,4,5 ,7 | H 03 D 3/00 H 03 G 3/20 |
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| A,D | PATENT ABSTRACTS OF JAPAN, vol. 7, no. 251 (E-209)[1396], 8th November 1983; & JP-A-58 137 309 (NIPPON DENKI K.K.) 15-08-1983 * Abstract * | 1,2,4,7 | |
| | | | TECHNICAL FIELDS SEARCHED (Int. CL 4) |
| | | | H 03 D H 03 G H 04 L |
| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 30-01-1989 | Examiner BALBINOT H. |
| CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document | | | |

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